Shonkho Shuvro

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ABOUT

Self motivated and ready to advance professional knowledge with excellent planning and problem-solving abilities. Prepared to implement diverse skill sets, technical proficiency, and new perspectives to leadership personnel.

AWARDS

Gold Medalist in B.Tech (ECE),
Mizoram University (A Central University)
17th March 2020

Second Position in Swacch Bharat Summer Internship Program, *Government of India*
26th March 2019

Subject Topper in Class XII (Computer Applications),
Rajendra Vidyalaya
7th August 2015

EDUCATION

Indian Institute of Science (Centre for NanoScience & Engineering), *Ph.D. (Nano Science & Engineering)*
July 2021 – present | Bengaluru, India

IIEST, Shibpur (Institute of National Importance),
M.Tech (VLSI Design)
July 2019 – July 2021 | Howrah, India
CGPA : 9.91

Mizoram University (A Central University),
B.Tech (Electronics & Communication Engg.)
2019 | Aizawl, India
CGPA : 9.42

Rajendra Vidyalaya, *Class XII (ICSE, Pure Science)*
2015 | Jamshedpur, India
Percentage: 91.00%

J.H. Tarapore School, *Class X (ICSE, Pure Science)*
2013 | Jamshedpur, India
Percentage: 86.20%

SKILLS

- Sentaurus TCAD
- MATLAB
- Origin
- VLSI

TEST

GATE 2019 (Electronics & Communication Engg.), *Qualified*
Score : 411

PUBLICATIONS

Analytical Modeling and FEM Simulation of the Collapse Voltage of an Angular Ring Metallization-Based MEMS Ultrasonic Transducer, *Proceedings of ICDMC (Springer)*
2nd June 2020
DOI : https://doi.org/10.1007/978-981-15-3631-1_18

Collapse Voltage analysis of Central Annular Ring Metallized Membrane Based MEMS Micromachined Ultrasonic Transducer, *Microsystem Technologies (Springer)*
4th September 2019
DOI : https://doi.org/10.1007/s00542-019-04613-x

Design and analysis of collapse voltage of Central Angular Ring metallization of MEMS based Micromachined Ultrasonic Transducer, *Applied Computer Technology Kolkata*
6th July 2019
Proceedings of 6th Int. Conf. MICRO, vol. 2, pp. 93-98, July-2019.

Effect of Electrode Area on Collapse Voltage of Micro-Electro-Mechanical System Based Micromachined Ultrasonic Transducer, *Applied Computer Technology, Kolkata*
29th December 2018
Proceedings of 1st Int. Conf. ESDA , pp. 17-22, Dec.2018

PROJECTS

M.Tech Project: Design, Optimization and Scaling of Thin-Body SOI Capacitor-less DRAM Cell,
(GlobalFoundries, Bangalore)
February 2020 – present
In this project, the capacitor-less 1T DRAM employs a floating body effect with the help of SOI technology as it has numerous benefits as compared to Bulk CMOS technology. We are using GIDL for low-power applications to store the charges within the body transistor without the need for a capacitor.

Design, Optimization and Scaling of Triple Well Bulk CMOS Capacitor-less DRAM Cell, *(GlobalFoundries, Bangalore)*
February 2020 – present
Here we propose Capacitor-less DRAM which is realized using Bulk CMOS Technology. This technology is the cheapest and most robust technology in terms of process/integration maturity. Low self-heating and ease of integration modules, make this technology popular among system designers. Using Triple Well Technology this capacitor-less DRAM is realized and using GIDL we are storing the charges.

B.Tech Project: MEMS based Capacitive 'MUT'
August 2018 – June 2020
Here we have analyzed the collapse voltage of CMUT by changing the electrode pattern, it's area, membrane thickness and it's material. We have also varied the gap height to see variations in collapse voltage. It is found that silicon carbide has got the least collapse voltage whereas diamond has got the highest collapse voltage. The annual ring metallization pattern is the best metallization pattern for CMUT.

CONFERENCES / SEMINARS / WORKSHOPS

- IEEE 4th International Test Conference India Organized by: IEEE Bangalore Section | Date: July, 2020
- "6th International Conference on Electronics, Computing & Communication Technologies", IEEE CONNECT , Organized by: IEEE Bangalore Section | Date: July, 2020
- "The Future of World Electronics and Possible Roles India Can Play",Organized by: IEEE Bangalore Section | Date: June, 2020
- "Role of Channel State Information in Adaption & Resource Allocation in Next Generation Wireless Systems" and "Wide Band Gap Semiconductor: Past, Present & Future" , Organized by: Dept. of Electronics & Communication Engineering, Mizoram University | Date : June 2020
- "3rd International Symposium on Devices, Circuits & Systems", Organized by: IIEST, Shibpur, Hiroshima University | Date : March,2020
- "The 28th IEEE Asian Test Symposium", Organized by: IIEST Shibpur, IIT Kharagpur, Calcutta University, Jadavpur University | Date: December, 2019
- "13th Instruction Enhancement Programme (IEP) Workshop Under SMDP-C2SD Project",Meity, GoI, Organized by: IIEST, Shibpur & Government of India | Date: August 2019
- "6th International Conference on Microelectronics, Circuits & Systems", Organized by : Amity University, Kolkata in association with Applied Computer Technology, Kolkata | Date: July 2019
- "International Conference on Design, Materials, Cryogenics & Construction", Organized by: Vel Tech Ragaranjan Dr. Sangunthala R&D Institute of Science & Technology | Date: March 2019
- "National Workshop on Emerging Trends in High Frequency Devices and Communication Technology" , Organized by: Mizoram University in collaboration with Mizoram University Incubation Center | Date: March 2019
- "First International Conference on Energy Systems Drives & Automations" , Organized by: Applied Computer Technology, Kolkata | Date: Decemeber 2018

ORGANISATIONS

J. H.Tarapore School - India, *Teaching the underprivileged*
April 2012 – June 2012 | Jamshedpur, India
Under a social help venture, my friends and I taught the students of Tarapore Balika Vidhyalaya (a school for the underprivileged).

EDU-CARE (NGO), *Poverty Allevation*
May 2008 – June 2008 | Jamshedpur, India
Voluntary contribution to poor people.

PROFESSIONAL EXPERIENCE

Student Intern, *NIELIT Calicut (In association with NIT Calicut)*
September 2020 – October 2020 | Calicut, India
I gained knowledge about the Industry Standard VLSI Design covering Analog and Digital Design flows and design methodologies. Starting with MOSFET models, CMOS Inverters, Op Amp, RTL and finally to GDS II file.

Student Intern, *CoreEL Technologies*
August 2020 – September 2020 | Bengaluru, India
In this entry-level position, I picked up the information on ASIC Physical Design Verification utilizing Industry Standard Mentor Graphics EDA tools. A portion of the themes learned to incorporate design difficulties in transistor model, different Analyses on transistor model like transient, DC and AC analysis, issues of Place and Route in full customs designs and verification strategies utilizing signoff Caliber instrument.

Student Intern, *Indian Railways*
June 2017 – July 2017 | Jamshedpur, India
Here I leaned about the different types of optical fibres and their specifications that are used in Indian Railways. I was also exposed to different types optical fibre communications that are used including how to join optical fibres (Splicing and using Connectors), what are different instruments which are used to determine the delay, power loses etc.

LANGUAGES

English
Hindi
Bengali

INTERESTS

- Painting
- Reading Books
- Listening to Music